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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


*Effective on 12/08/2004.*
*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).*

# FEE TRANSMITTAL
## For FY 2009

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 540.00

| Complete if Known | |
|---|---|
| Application Number | 10/525,203-Conf. #7661 |
| Filing Date | February 22, 2005 |
| First Named Inventor | Yuichi Takagi |
| Examiner Name | D. P. Joseph |
| Art Unit | 2629 |
| Attorney Docket No. | SON-2815 |

**METHOD OF PAYMENT** (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 18-0013 Deposit Account Name: Rader, Fishman & Grauer PLLC

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

**FEE CALCULATION**

**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

| | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | |
|---|---|---|---|---|---|---|---|
| Application Type | Fee ($) | Small Entity Fee ($) | Fee ($) | Small Entity Fee ($) | Fee ($) | Small Entity Fee ($) | Fees Paid ($) |
| Utility | 330 | 165 | 540 | 270 | 220 | 110 | |
| Design | 220 | 110 | 100 | 50 | 140 | 70 | |
| Plant | 220 | 110 | 330 | 165 | 170 | 85 | |
| Reissue | 330 | 165 | 540 | 270 | 650 | 325 | |
| Provisional | 220 | 110 | 0 | 0 | 0 | 0 | |

**2. EXCESS CLAIM FEES**

| Fee Description | Fee ($) | Small Entity Fee ($) |
|---|---|---|
| Each claim over 20 (including Reissues) | 52 | 26 |
| Each independent claim over 3 (including Reissues) | 220 | 110 |
| Multiple dependent claims | 390 | 195 |

| Total Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - or HP = | _____ | x _____ | = _____ |

HP = highest number of total claims paid for, if greater than 20.

| Indep. Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - or HP = | _____ | x _____ | = _____ |

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims — Fee ($): _____ Fee Paid ($): _____

**3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | Extra Sheets | Number of each additional 50 or fraction thereof | Fee ($) | Fee Paid ($) |
|---|---|---|---|---|
| _____ - 100 = | _____ | /50 = _____ (round up to a whole number) x | _____ | = _____ |

**4. OTHER FEE(S)** Fees Paid ($)

Non-English Specification, $130 fee (no small entity discount)

Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal 540.00

**SUBMITTED BY**

| | | | | | |
|---|---|---|---|---|---|
| Signature | 40,290 | Registration No. (Attorney/Agent) | 40,290<br>24,104 | Telephone | (202) 955-3750 |
| Name (Print/Type) | Christopher M. Tobin<br>Ronald P. Kananen | | | Date | February 23, 2009 |

# TRANSMITTAL OF APPEAL BRIEF

Docket No.
SON-2815

In re Application of: Yuichi Takagi et al.

| Application No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| 10/525,203-Conf. #7661 | February 22, 2005 | D. P. Joseph | 2629 |

Invention: CURRENT OUTPUT TYPE DRIVE CIRCUIT AND DISPLAY DEVICE

**TO THE COMMISSIONER OF PATENTS:**

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: October 22, 2008 .

The fee for filing this Appeal Brief is $ 540.00 .

[x] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[ ] A check in the amount of _____ is enclosed.

[x] Charge the amount of the fee to Deposit Account No. 18-0013 .

[ ] Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 18-0013 .
This sheet is submitted in duplicate.

40,290

Dated: February 23, 2009

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Docket No.: SON-2815

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Yuichi Takagi et al.

Application No.: 10/525,203 | Confirmation No.: 7661

Filed: February 22, 2005 | Art Unit: 2629

For: CURRENT OUTPUT TYPE DRIVE CIRCUIT AND DISPLAY DEVICE | Examiner: D. P. Joseph

# APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal Brief under 37 C.F.R. § 41.37 appealing the Final Office Action of the Examiner dated July 25, 2008. This Brief is also in furtherance of the Notice of Appeal previously filed on October 22, 2008 along with a Request for Pre-Appeal Brief Panel Review. A Panel Decision dated January 21, 2009 allowed this matter to proceed to the Board of Patent Appeals and Interferences.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:



## I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Sony Corporation, of Tokyo, Japan. An assignment of all rights in the present application to Sony Corporation was executed by the inventors and recorded by the United States Patent and Trademark Office at Reel 016993, Frame 0699.

## II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

## III. STATUS OF CLAIMS

### A. Current Status of Claims

A complete listing of the claims with corresponding status is provided as follows:

Claims 1-28. (Rejected).

### B. Claims On Appeal

Appellant hereby appeals the final rejection of claims 1-28.

## IV. STATUS OF AMENDMENTS

A Non-Final Office Action rejecting claims 1-28 was mailed on May 5, 2008 October 31, 2007 and a Request for Reconsideration was filed on April 23, 2008 requesting reconsideration of the rejected claims. A Final Office Action rejecting claims 1-28 was mailed on July 25, 2008. Another Request for Reconsideration was then filed on September 22, 2008, and an Advisory Action dated October 2, 2008 maintained the grounds of rejection. Appellant then filed a Notice of Appeal and Request for Pre-Appeal Brief Panel Review on October 22, 2008. A Decision on Panel Review dated January 21, 2009 allowed the matter to proceed to the Board of Patent Appeals and Interferences.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

References to the specification and drawings are made below to illustrate an example of the claimed invention in summary form. Reference to a figure or portion of text does not constitute an indication or admission that the cited passage and/or figure is the only example in Appellant's application as filed. Additionally, these citations are for illustrative purposes and are not intended to limit the scope of the invention.

Independent claim 1 recites: [a] current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas (*e.g.*, FIG. 4, page 14, line 15 through page 19, line 20; FIG. 6; FIG. 22, page 72, line 3 through page 75, line 15),

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object (e.g., FIG. 4, 101-1, 101-2, 101-3, p. 14, lines 19-23; FIG. 6, page 22, line 13 through page 23, line 23; FIG. 22)

each driver comprising

an output means (FIG. 6, 900-1, 900-2, 900-3, FIG. 16, 900) for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object (FIG. 6, 900-1, 900-2, 900-3, page 22, lines 15-24; FIG. 16, page 53, line 11 through page 56, line 14) and

a reference current source circuit (FIG. 6, 200; FIGs. 7-9; FIG. 15) for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means (FIG. 6, 200, page 22, line 25 through page 23, line 23; FIGs. 7-9, page 23, line 24 through page 44, line 23).

Dependent claim 3 recites: [a] current output type drive circuit as set forth in claim 2, wherein

said current sampling circuit includes a first current memory and a second current memory (FIG. 8, FIG. 9, 2021, 2022; page 27, line 9 through page 31, line 1), and

said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory (page 27, line 9 through page 31, line 1; page 33, line 25 through page 35, line 22).

Dependent claim 4 recites: [a] current output type drive circuit as set forth in claim 2, wherein said output means includes a plurality of current output type digital/analog conversion circuits and

the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits (*e.g.*, FIG. 6, page 22, line 25 through page 23, line 7).

Dependent claim 5 recites: [a] current output type drive circuit as set forth in claim 4, wherein

each driver is a driver outputting currents of a plurality of channels in accordance with input data,

further comprises a register array for holding said input data (FIG. 6, 600; page 22, line 12 through page 23, line 23), and

further comprises means for increasing the reference current sampled and held by the reference current source circuit to a plurality of reference currents by further copying or distributing them by time division (*e.g.*, FIG. 6, page 22, line 25 through page 23, line 7), and

said output means comprises

a plurality of conversion circuits for receiving said plurality of reference currents and outputting currents in accordance with the data held by the register array (FIG. 6, 800-1 through m; page 22, line 12 through page 23, line 23) and

a current output circuit comprising a first group of current sampling circuits and a second group of current sampling circuits operating alternately in a current write mode and current read mode in accordance with the output currents of the conversion circuits (FIG. 16, 901-1 through 901-n and 902-1 through 902-n; page 53, line 11 through page 56, line 14) .

Dependent claim 6 recites: [a] current output type drive circuit as set forth in claim 5, wherein

said input data is digital image data,

the circuit comprises means for distributing the reference current to the drivers in a vertical blanking period during which operations on said image data are suspended (FIG. 13A-13H; page 43, line 5 through page 44, line 23), and

each driver uses as the reference current the current held in the reference current source circuit of the driver after the vertical blanking period in which digital noise is generated along with transfer of said image data (FIG. 13A-13H; page 43, line 5 through page 44, line 23).

Independent claim 7 recites: [a] current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas (*e.g.*, FIG. 4, page 14, line 15 through page 19, line 20; FIG. 6; FIG. 22, page 72, line 3 through page 75, line 15),

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object (e.g., FIG. 4, 101-1, 101-2, 101-3, p. 14, lines 19-23; FIG. 6, page 22, line 13 through page 23, line 23; FIG. 22),

each driver comprising

an output means for outputting a supplied reference current as a drive current to the corresponding shared area of the driven object (FIG. 6, 900-1, 900-2, 900-3, page 22, lines 15-24; FIG. 16, page 53, line 11 through page 56, line 14) and

a reference current source circuit for sampling and holding a reference current input from a reference current input terminal, then supplying the same to the output means (*e.g.*, FIG. 6, 200, page 22, line 25 through page 23, line 23; FIGs. 7-9, page 23, line 24 through page 44, line 23),

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect (*e.g.*, FIG. 4, CML1, page 16, lines 8-20), and

the reference current being distributed to the reference current source circuits of the drivers by time division (*e.g.*, FIG. 6, page 22, line 25 through page 23, line 7).

Independent claim 22 recites: [a] display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas (*e.g.*, FIG. 4, page 14, line 15 through page 19, line 20; FIG. 6; FIG. 22, page 72, line 3 through page 75, line 15),

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel (FIG. 6, 900-1, 900-2, 900-3, page 22, lines 15-24; FIG. 16, page 53, line 11 through page 56, line 14),

each driver comprising an output means for outputting a supplied reference current to a corresponding shared area of the driven object (FIG. 6, 900-1, 900-2, 900-3, page 22, lines 15-24; FIG. 16, page 53, line 11 through page 56, line 14) and

a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means (*e.g.*, FIG. 6, 200, page 22, line 25 through page 23, line 23; FIGs. 7-9, page 23, line 24 through page 44, line 23).

Independent claim 23 recites: [a] display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas (*e.g.*, FIG. 4, page 14, line 15 through page 19, line 20; FIG. 6; FIG. 22, page 72, line 3 through page 75, line 15),

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel (FIG. 6, 900-1, 900-2, 900-3, page 22, lines 15-24; FIG. 16, page 53, line 11 through page 56, line 14),

each driver comprising

an output means for outputting a supplied reference current to a corresponding shared area of the driven object (FIG. 6, 900-1, 900-2, 900-3, page 22, lines 15-24; FIG. 16, page 53, line 11 through page 56, line 14) and

a reference current source circuit for sampling and holding a reference current input from a reference current input terminal, then supplying the same to the output means (*e.g.*, FIG. 6, 200, page 22, line 25 through page 23, line 23; FIGs. 7-9, page 23, line 24 through page 44, line 23),

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect (*e.g.*, FIG. 4, CML1, page 16, lines 8-20), and

the reference current being distributed to the reference current source circuits of the drivers by time division (*e.g.*, FIG. 6, page 22, line 25 through page 23, line 7).

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal, with separate arguments as noted in the following sections, are as follows:

Whether the Examiner erred in rejecting claims 1-28 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,332,661 to Yamaguchi ("Yamaguchi") in view of U.S. Pat. No. 7,180,496 to Koyama et al. ("Koyama").

These issues are discussed in the following section, with subsections corresponding to the separate arguments.

## VII. ARGUMENT

### VII.A Introduction.

In the Final Office Action of May 30, 2008, the Examiner erred in rejecting claims 1-28 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi in view of Koyama. Consistent with the grouping of claims in the following sections, these rejections are variously deficient as noted in the separate arguments.

### VII.B Yamaguchi and Koyama fail to disclose or suggest the features recited in independent claims 1 and 22.

Claim 1 recites: *[a] current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas,*

*comprising a plurality of drivers arranged corresponding to each the shared area of the driven object, each driver comprising*

*an output means for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object and*

*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.*

These claimed features are neither disclosed nor suggested by the relied-upon references. Yamaguchi discloses a constant current driving semiconductor integrated circuit configured to drive several loads by using a reference current generating circuit that is embedded to derive a reference output current generated on a reference resistance from a reference output terminal. This provides constant current driver ICs that are intended to operate in a state of small variations in output currents. Appellant submits that this arrangement is similar to the problematic examples described in Appellant's background of the invention, and is clearly distinct from and not suggestive in any way of Appellant's claimed invention.

There are thus various claimed features that are absent from Yamaguchi. For example, the Final Office Action readily admits that, and Yamaguchi makes no mention of, "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means*," as claimed by Appellant.

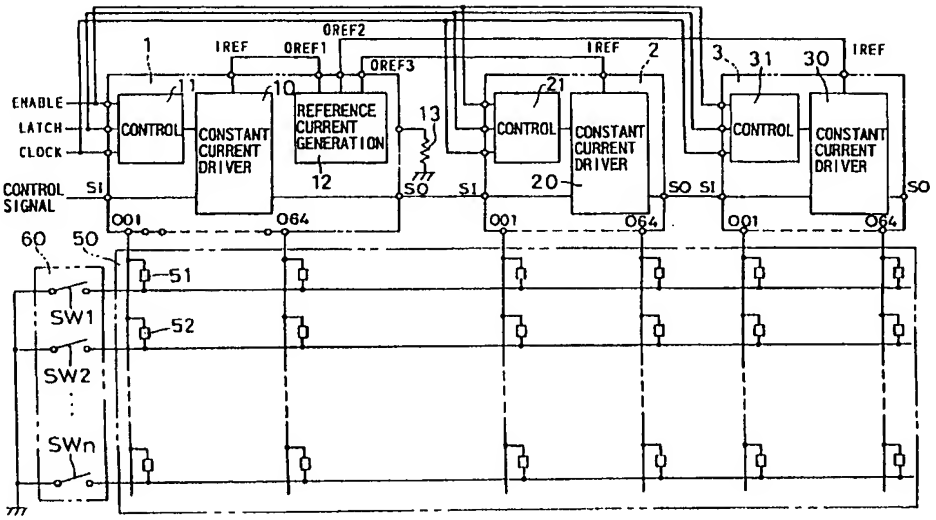
Koyama does not remedy the deficiencies of Yamaguchi. Koyama discloses a drive circuit for driving a liquid crystal display device. Koyama discloses a line driver circuit that outputs digital values (D1, D2, D3) to the pixel array in the form of a voltage. This digital line driver circuit of Koyama fails to even generally disclose the type of circuit claimed by Appellant, which is a "*current output type drive circuit for outputting a drive current ...comprising a plurality of drivers*

*... for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object.*"

Moreover, like Yamaguchi, Koyama clearly fails to disclose or suggest "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means*," as claimed by Appellant. The Final Office Action cites FIG. 2, elements 201 and 202 as a purported example of this feature. However, these elements merely accommodate a latching of a digital signal (D1, D2, D3) that is then provided to a pixel circuit 205. At best, even if this is construed as "sampling" and "holding", the passing of a digital value D1, D2, or D3 to another circuit is clearly not an example of sampling a reference current input from a reference current input terminal. The passage cited in the Final Office Action (9:21-25) merely confirms that Koyama samples digital data, and in no way discloses or in any way suggests a reference current source circuit that samples and holds the reference current input from a reference current input terminal, and then supplies the same to the output means.

Additionally, and contrary to the conclusory remarks of the Examiner that sampling and holding signals is a known technique and that this combination would have been obvious, one of ordinary skill in the art would not have combined the claimed elements by known methods as there would be no technical impetus whatsoever to make the modifications consistent with Appellant's claimed invention, and there would thus also be no expectation that success would result in adding such features to the circuitry of Yamaguchi.

FIG. 1 of Yamaguchi illustrates the current driving circuitry disclosed therein:




Yamaguchi also describes circuitry that provides a current mirror circuit including transistors configured to produce reference current outputs OREF1-3 that have small variations in current value. (See FIG. 3 of Yamaguchi). It would make no technical sense whatsoever to sample and hold these currents in the Yamaguchi circuitry, as these currents are intended to drive loads (with the alleged small variation in current). If one were to sample and hold the OREF1-3 currents, in lieu of using them to drive loads, the circuitry would be rendered completely non-functional.

The reference to FIG. 2 of Yamaguchi (Office Action, at p. 21) as further evidence of the propriety of the combination only further highlights the specious nature of the rejection. Although the explanation in the reference is scant, the register and latch disclosed therein are apparently control circuitry used to determine which line the drive current is to be applied to. This has nothing to do with sampling or holding the value of the actual current.

Accordingly, Yamaguchi discloses circuitry for producing several drive currents with small variation, and Koyama discloses an entirely different type of circuit and fails to disclose or in any way suggest the claimed features that the Final Office Action admits are absent from the Yamaguchi reference. The line (voltage) driver circuit by Koyama is a clearly distinct from the current driver circuit claimed by Appellant. Additionally, as noted above, there would be absolutely no reason to even consider sample and hold circuitry in the Yamaguchi circuitry. An ordinarily

skilled artisan would in no way look to the latching of a digital value (D1-D3) for application to a line in a pixel circuit to solve problems presented in the current drive circuitry of Yamaguchi. Regardless, a *prima facie* case of obviousness remains absent from the record as even the combination of references would still fail to yield the features of Appellant's claimed invention, namely "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.*"

The Advisory Action alleges that Appellant did not seem to argue the Yamaguchi reference, but more the Koyama reference and specifically the combination. Appellant believes that the above quite clearly addresses the deficiencies or Yamaguchi, as well as Koyama, as well as the faulty combination. Appellant also wishes to note that the claimed invention is not merely the introduction of a "sample and hold circuit" into a circuit of the type disclosed by Yamaguchi. Appellant submits that the Final Office Action and Advisory Action improperly seek to distill the differences between what is claimed, and what is disclosed by the prior art in this fashion.

The Advisory Action also now cites to column 6, lines 46-64 of Yamaguchi as supposed evidence of a sample and hold circuit. However, this is only further indication of the impropriety of the rejection. The cited passage merely states that a 64 bit latch (80) may capture and hold data from the shift register (70). This is clearly distinct from "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means*," as claimed by Appellant, and is another example of a lack of appreciation of the actual claim language and the context of this feature of the claimed invention.

For these reasons, the combination of references is thus deficient generally, and the faulty combination still fails to produce the features recited in Appellant's claim 1. Claim 1 is clearly distinct from the relied upon references, whether they are taken alone or in any combination. Independent claim 22 is distinct from the relied upon references for reasons similar to those provided regarding claim 1.

Accordingly, Appellant respectfully requests reversal of the rejection of independent claims 1 and 22.

VII.C Yamaguchi and Koyama fail to disclose or suggest the features recited in dependent claim 3.

Dependent claim 3 recites: ... *said current sampling circuit includes a first current memory and a second current memory, and said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory.*

The Final Office Action alleges that Koyama discloses these features, and cites elements A1 to A3 and B1 to B3 as the first current memory and elements C1 to C3 as the second current memory. However, as noted, these elements are part of the pixel, not a part of the line drive circuit.

It is clear that these features are not an example of first and second current memories in a current sampling circuit, let alone those that alternately perform write and read operations as claimed. Again, Appellant's claimed invention provides two memory circuits to write and read the reference current in the reference current source circuit, not within the pixel array. The second current memory in Yamaguchi C1-C3 is merely a non-volatile memory that stores the values in the given pixel when power to the display is cut off, so that the display can automatically display something when it is turned back on. The other elements A1 to A3 and B1 to B3 are merely faster, volatile memories for accommodating a refresh of the display. It is difficult to see how the cited features of Koyama have anything at all to do with the features recited in Appellant's claim 3.

It is not a mere "design choice" as alleged in the Advisory Action, where Appellant has specifically claimed two distinct current memories along with "*alternately perform[ing] a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory.*" As was the pattern with the independent claim, the Action points to a wholly out of

context example of two memories in a completely different portion of the circuitry, that in no way discloses or in any way suggests the clearly claimed features of Appellant's invention.

Accordingly, Appellant respectfully requests reversal of the rejection of claim 3 and any similar claims.

VII.D Yamaguchi and Koyama fail to disclose or suggest the features recited in dependent claims 4 and 5.

Dependent claim 4 recites: *[a] current output type drive circuit as set forth in claim 2, wherein said output means*

*includes a plurality of current output type digital/analog conversion circuits and*

*the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and*

*said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits.*

Dependent claim 5 recites: *[a] current output type drive circuit as set forth in claim 4, wherein*

*each driver is a driver outputting currents of a plurality of channels in accordance with input data,*

*further comprises a register array for holding said input data, and*

*further comprises means for increasing the reference current sampled and held by the reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and*

*said output means comprises*

*a plurality of conversion circuits for receiving said plurality of reference currents and outputting currents in accordance with the data held by the register array and*

*a current output circuit comprising a first group of current sampling circuits and a second group of current sampling circuits operating alternately in a current write mode and current read mode in accordance with the output currents of the conversion circuits.*

With regard to claim 4, the relied-upon references offer no disclosure or suggestion of means for increasing the reference current read from the current memory via distribution by time division. It is not sufficient to state that time division is known, as there would be no reason to distribute reference currents by time division in the Yamaguchi reference.

With regard to claim 5, there is clearly no disclosure or suggestion of the additional features for carrying out such an operation as clamed, in particular "*a current output circuit comprising a first group of current sampling circuits and a second group of current sampling circuits operating alternately in a current write mode and current read mode in accordance with the output currents of the conversion circuits.*"

Appellant objects to the unsupported conclusory statements that these claimed features are obvious. Accordingly, Appellant respectfully requests reversal of the rejection of claims 4 and 5, and any similar claims.

VII.E Yamaguchi and Koyama fail to disclose or suggest the features recited in dependent claim 6.

Dependent claim 6 recites: *[a] current output type drive circuit as set forth in claim 5, wherein*

*said input data is digital image data,*

*the circuit comprises means for distributing the reference current to the drivers in a vertical blanking period during which operations on said image data are suspended, and*

*each driver uses as the reference current the current held in the reference current source circuit of the driver after the vertical blanking period in which digital noise is generated along with transfer of said image data.*

With regard to claim 6, there is also absolutely no discussion in Yamaguchi, as alleged in the Final Office Action, of distributing the reference current to the drivers in a vertical blanking period, or of using as the reference current the current held after the vertical blanking period in which digital noise is generated, as claimed by Appellant. Even assuming that Yamaguchi column 6, lines 22-45 discloses the usage of clock signals to control displayed information, there is no mention or suggestion of any kind of distributing the reference current to the drivers in a vertical blanking period. It would also make no sense to do this in Yamaguchi as that circuitry provides drive currents for driving loads. There is no way one would in any way consider that it would be "inherent" to distribute the reference current in a vertical blanking period, as this would be non-functional in the Yamaguchi reference. Appellant objects to the unsupported conclusory statement that these claimed features would have been obvious.

Accordingly, Appellant respectfully requests reversal of the rejection of claim 6, and any similar claims.

VII.F Yamaguchi and Koyama fail to disclose or suggest the features recited in independent claims 7 and 23.

Independent claim 7 recites: *[a] current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas,*

*comprising a plurality of drivers arranged corresponding to each the shared area of the driven object,*

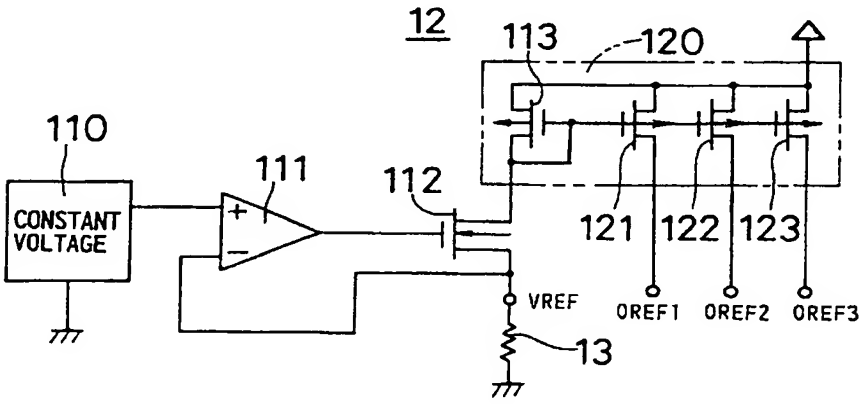
*each driver comprising an output means for outputting a supplied reference current as a drive current to the corresponding shared area of the driven object and a reference current source circuit for sampling and holding a reference current input from a reference current input terminal, then supplying the same to the output means,*

*the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect, and*

*the reference current being distributed to the reference current source circuits of the drivers by time division.*

Claim 7 is distinct from the relied-upon references for the reasons noted regarding claim 1 above. Additionally, there is no disclosure or suggestion in the relied upon references of (1) connecting the reference current inputs according to a common current interconnect, or of (2) distributing the reference current to the reference current source circuits of the drivers by time division. As explained above, Yamaguchi discloses a reference current generating circuit that is embedded to derive a reference output current generated on a reference resistance from a reference output terminal. FIG. 3 of Yamaguchi discloses its reference current generating circuit, which is explicitly described as producing different currents for the different current driver circuits.

FIG. 3




This is not an example of the common current interconnect claimed by Appellant. In any event, there is clearly no distribution of the reference current to the reference current source circuits of the drivers by time division, nor is there anything that could coherently support a conclusion that there is any hint or suggestion in that regard.

The use of time division appears wholly inappropriate to the circuitry of Yamaguchi, and it is unclear how or if Yamaguchi's drive circuitry would function under such a scenario. In any case, there is clearly no indication whatsoever that time division would be used in the context or fashion claimed by Appellant. It is wholly insufficient to merely conclude that time division is known, and that therefore it would be obvious. Koyama also fails to disclose or in any way suggest such features. The passage cited in the Final Office Action, spanning lines 1-21 in column 10, discloses a gray scale technique, which also clearly does not disclose or suggest the claimed features.

Claim 23 is distinct for at least reasons similar to those provided regarding claim 7 above.

Any remaining claims depend from these claims and are thus distinct for incorporating the features therein as well as for their separately recited, distinct features, some of which are specifically addressed above.

For the foregoing reasons, Appellant respectfully requests reversal of the Examiner's rejection of claims 1-28 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi in view of Koyama.

## VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

## IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132, or additional evidence entered by or relied upon by the Examiner is being submitted.

## X. RELATED PROCEEDINGS

No related proceedings are referenced in section II above, or copies of decisions in related proceedings are not provided.

**Conclusion**

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

Dated: Feb. 23, 2009

Respectfully submitted,

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## APPENDIX A - claims

1. A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas,

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object,

each driver comprising

an output means for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object and

a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.

2. A current output type drive circuit as set forth in claim 1, wherein said reference current source circuit comprises at least:

a current sampling circuit including a current memory for sampling and holding said reference current in accordance with a control signal and

a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit.

3. A current output type drive circuit as set forth in claim 2, wherein

said current sampling circuit includes a first current memory and a second current memory, and

said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory.

4. A current output type drive circuit as set forth in claim 2, wherein said output means includes a plurality of current output type digital/analog conversion circuits and

the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and

said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits.

5. A current output type drive circuit as set forth in claim 4, wherein

each driver is a driver outputting currents of a plurality of channels in accordance with input data,

further comprises a register array for holding said input data, and

further comprises means for increasing the reference current sampled and held by the reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and

said output means comprises

a plurality of conversion circuits for receiving said plurality of reference currents and outputting currents in accordance with the data held by the register array and

a current output circuit comprising a first group of current sampling circuits and a second group of current sampling circuits operating alternately in a current write mode and current read mode in accordance with the output currents of the conversion circuits.

6. A current output type drive circuit as set forth in claim 5, wherein

said input data is digital image data,

the circuit comprises means for distributing the reference current to the drivers in a vertical blanking period during which operations on said image data are suspended, and

each driver uses as the reference current the current held in the reference current source circuit of the driver after the vertical blanking period in which digital noise is generated along with transfer of said image data.

7. A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas,

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object,

each driver comprising

an output means for outputting a supplied reference current as a drive current to the corresponding shared area of the driven object and

a reference current source circuit for sampling and holding a reference current input from a reference current input terminal, then supplying the same to the output means,

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect, and

the reference current being distributed to the reference current source circuits of the drivers by time division.

8. A current output type drive circuit as set forth in claim 7, wherein each driver fetches said reference current from said reference current input terminal to said reference current source circuit when receiving a signal indicating start of distribution of the reference current and outputs the signal indicating the start of distribution of reference current to the driver circuit of the next stage.

9. A current output type drive circuit as set forth in claim 8, wherein each driver comprises a data memory, writes input data into said data memory when receiving a first signal indicating start of writing of data and outputs said first signal indicating start of writing of data to the driver of the next stage and fetches said reference current from said reference current input terminal to said reference current source circuit in synchronization with said first signal when receiving a second signal indicating start of distribution of reference current and outputs said second signal indicating start of distribution of reference current to the driver circuit of the next stage.

10. A current output type drive circuit as set forth in claim 7, wherein said reference current source circuit comprises at least:

a current sampling circuit including a current memory for sampling and holding said reference current in accordance with a control signal and

a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit.

11. A current output type drive circuit as set forth in claim 10, wherein

said current sampling circuit includes a first current memory and a second current memory, and

said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory.

12. A current output type drive circuit as set forth in claim 10, wherein said output means

includes a plurality of current output type digital/analog conversion circuits and

the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and

said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits.

13. A current output type drive circuit as set forth in claim 7, wherein at least the reference current source circuit of the driver serving as a master includes a reference current source circuit generating a reference current and supplying it to said common current interconnect.

14. A current output type drive circuit as set forth in claim 10, wherein at least the reference current source circuit of the driver serving as a master includes a reference current source circuit generating a reference current and supplying it to said common current interconnect.

15. A current output type drive circuit as set forth in claim 7, wherein

each driver is a driver outputting currents of a plurality of channels in accordance with input data,

further comprises a register array for holding said input data, and

further comprises means for increasing the reference current sampled and held by the reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and

said output means comprises

a plurality of conversion circuits for receiving said plurality of reference currents and outputting currents in accordance with the data held by the register array and

a current output circuit having a first group of current sampling circuits and a second group of current sampling circuits operating alternately in a current write mode and current read mode in accordance with the output currents of the conversion circuits.

16. A current output type drive circuit as set forth in claim 15, wherein

said input data is digital image data,

the circuit comprises means for distributing the reference current to the drivers in a vertical blanking period during which operations on said image data are suspended, and

each driver uses as the reference current the current held in the reference current source circuit of the driver after the vertical blanking period in which digital noise is generated along with transfer of said image data.

17. A current output type drive circuit as set forth in claim 7, wherein the interconnect of said reference current is arranged between power supply interconnects for shield.

18. A current output type drive circuit as set forth in claim 7, wherein the interconnect of said reference current, when a multilayer interconnect including a power supply layer for shield, is arranged at a top layer of said power supply layer for shield.

19. A current output type drive circuit as set forth in claim 7, further comprising means for suppressing great fluctuations of the potential of said common reference current interconnect when the circuits sampling and holding the reference currents of the drivers are all off.

20. A current output type drive circuit as set forth in claim 12, wherein

said means increasing said reference current to a plurality of reference currents comprises a current mirror circuit configured by a constant current source including resistor elements arranged at the input stage and a plurality of reference current sources including resistor elements arranged at the output stage in parallel so as to correspond to the output parts of said output means, and

the resistor elements of the reference current sources arranged at the two ends among said plurality of reference current sources are arranged close to the resistor elements of said constant current source.

21. A current output type drive circuit as set forth in claim 20, wherein the resistor elements forming the reference current sources are laid out divided and cross-laced.

22. A display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas,

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel,

each driver comprising an output means for outputting a supplied reference current to a corresponding shared area of the driven object and

a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.

23. A display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas,

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel,

each driver comprising

an output means for outputting a supplied reference current to a corresponding shared area of the driven object and

a reference current source circuit for sampling and holding a reference current input from a reference current input terminal, then supplying the same to the output means,

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect, and

the reference current being distributed to the reference current source circuits of the drivers by time division.

24. A display device as set forth in claim 23, wherein each driver fetches said reference current from said reference current input terminal to said reference current source circuit when receiving a signal indicating start of distribution of reference current and outputs the signal indicating start of distribution of reference current to the driver circuit of the next stage.

25. A display device as set forth in claim 23, wherein each driver comprises a data memory, writes input data into said data memory when receiving a first signal indicating start of writing of data and outputs said first signal indicating start of writing of data to the driver of the next stage and fetches said reference current from said reference current input terminal to said reference current source circuit in synchronization with said first signal when receiving a second signal indicating start of distribution of reference current and outputs said second signal indicating start of distribution of reference current to the driver circuit of the next stage.

26. A display device as set forth in claim 23, wherein the interconnect of said reference current is arranged between power supply interconnects for shield.

27. A display device as set forth in claim 23, wherein the interconnect of said reference current, when a multilayer interconnect including a power supply layer for shield, is arranged at a top layer of said power supply layer for shield.

28. A display device as set forth in claim 23, further comprising means for suppressing great fluctuations of the potential of said common reference current interconnect when the circuits sampling and holding the reference currents of the drivers are all off.

## APPENDIX B – ADDITIONAL EVIDENCE

None.

## APPENDIX C – RELATED PROCEEDINGS

None.